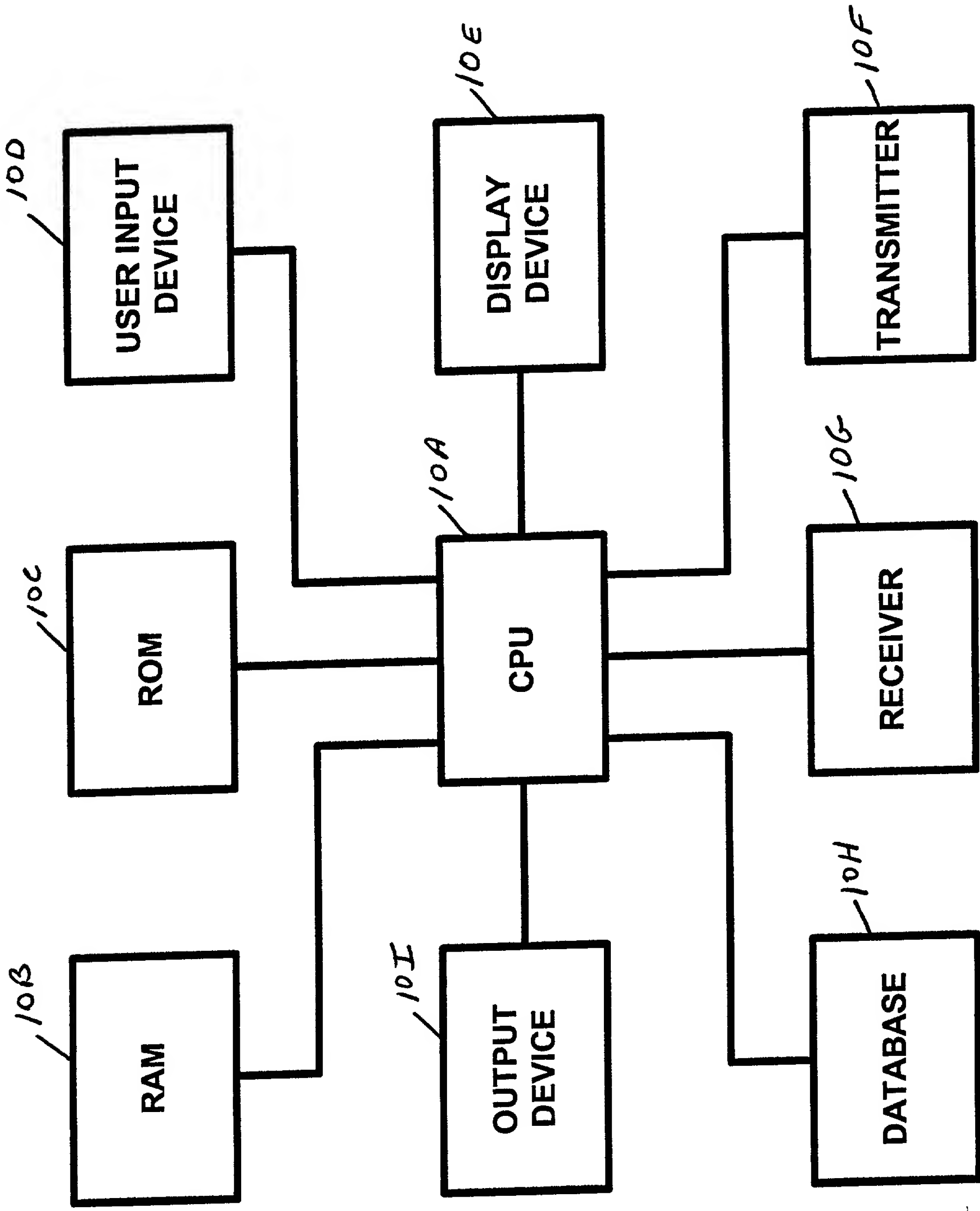


FIG. 1

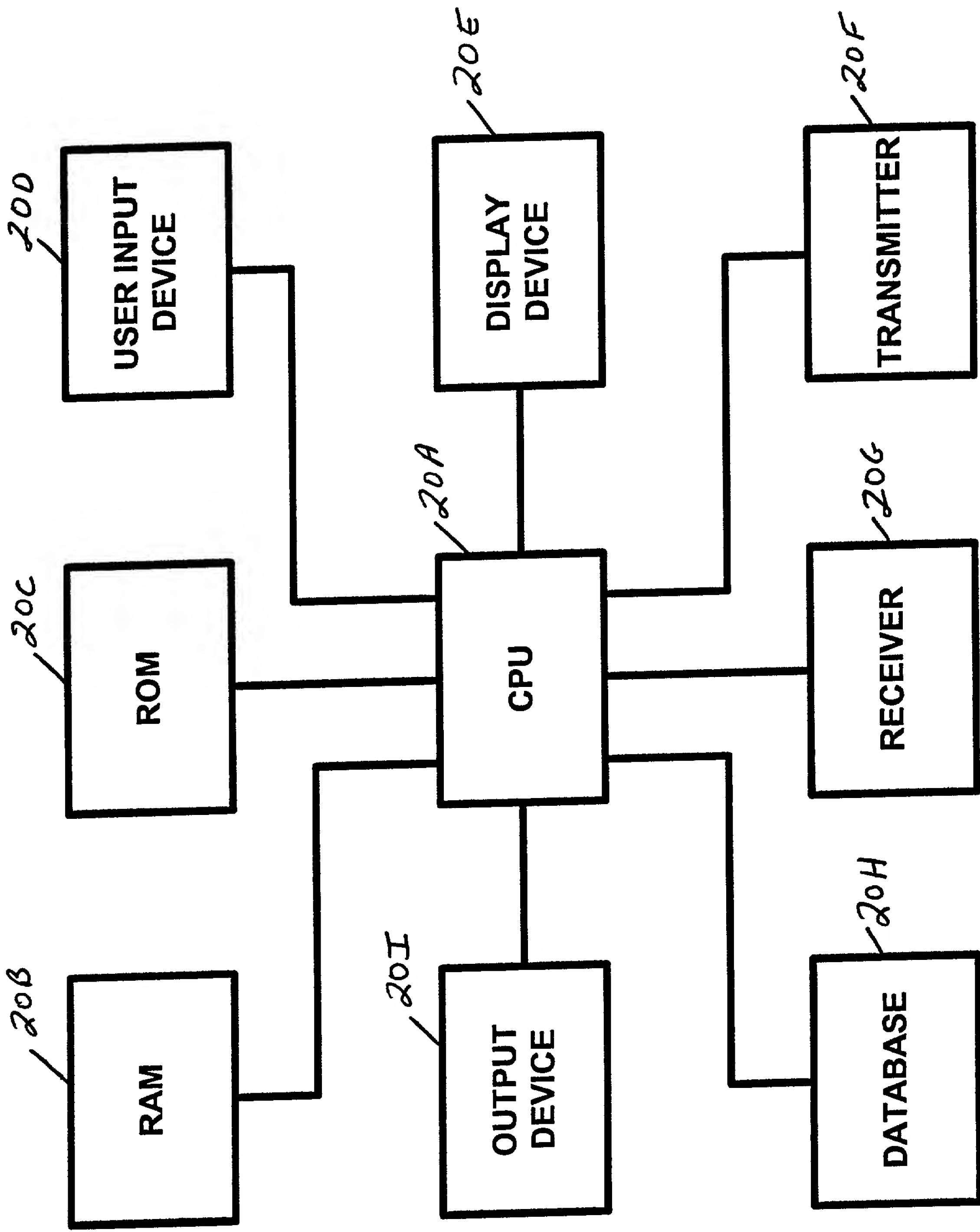
100-

FIG. 2 is a block diagram of a computer system 100. The system 100 includes a central processing unit (CPU) 10A, a random access memory (RAM) 10B, a read only memory (ROM) 10C, a user input device 10D, a display device 10E, a transmitter 10F, a receiver 10G, a database 10H, and an output device 10I. The CPU 10A is connected to the RAM 10B, the ROM 10C, the user input device 10D, the display device 10E, the transmitter 10F, the receiver 10G, the database 10H, and the output device 10I.



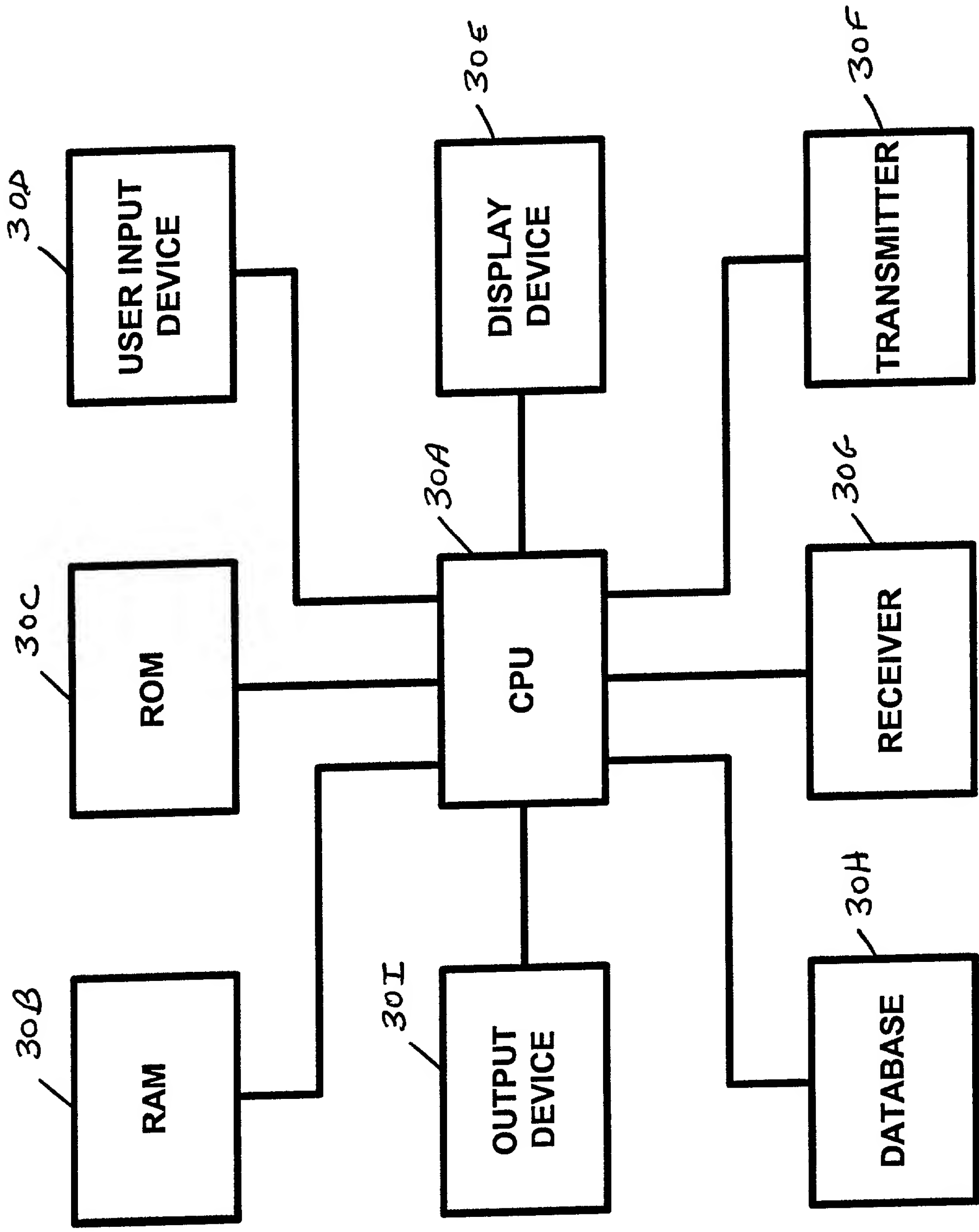
100-

FIG. 2



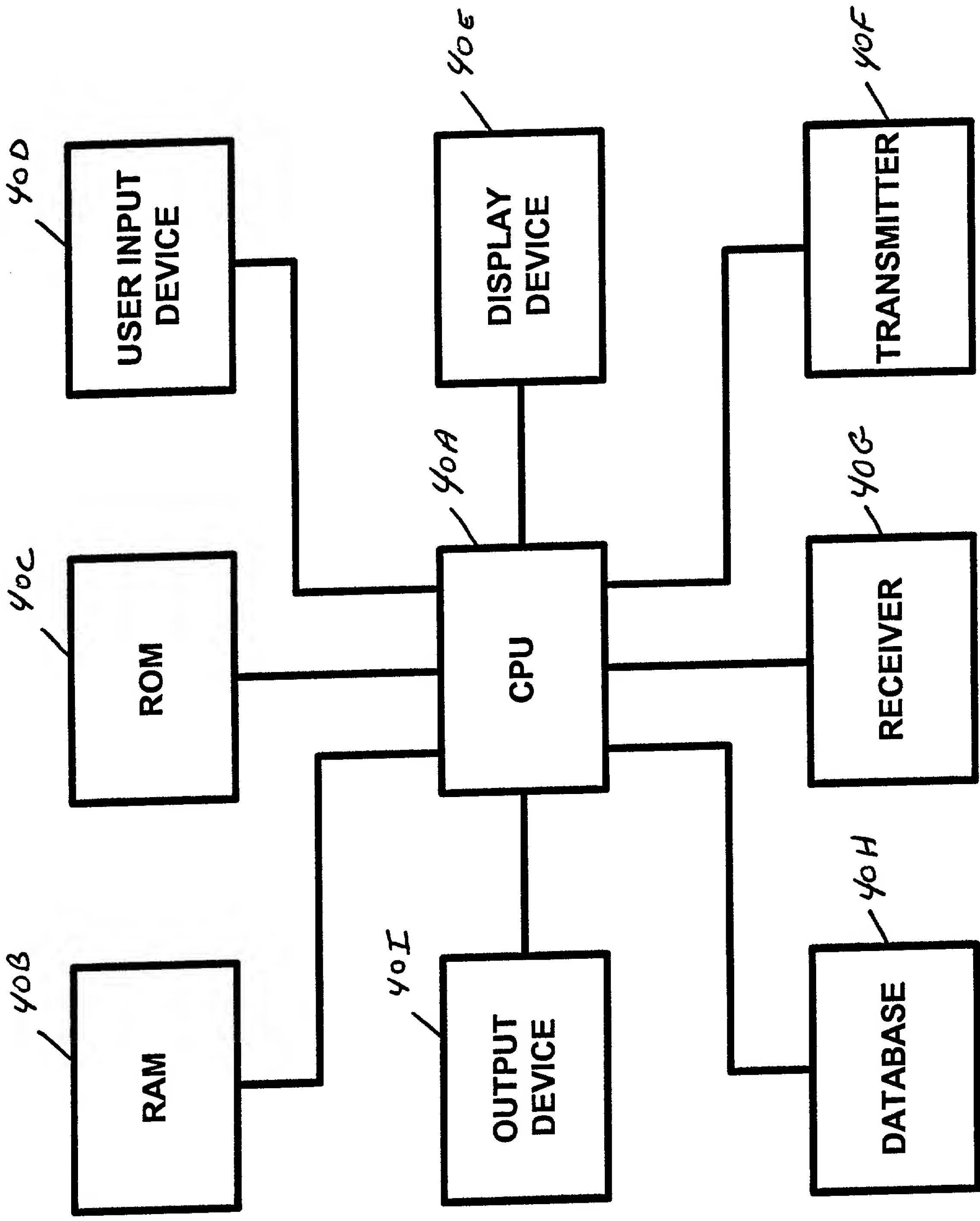
20-  
**FIG. 3**

FIG. 4 is a block diagram of a system 300 in accordance with the present invention. The system 300 includes a CPU 30A, a RAM 30B, a ROM 30C, a user input device 30D, an output device 30E, a display device 30F, a receiver 30G, a transmitter 30H, and a database 30I.



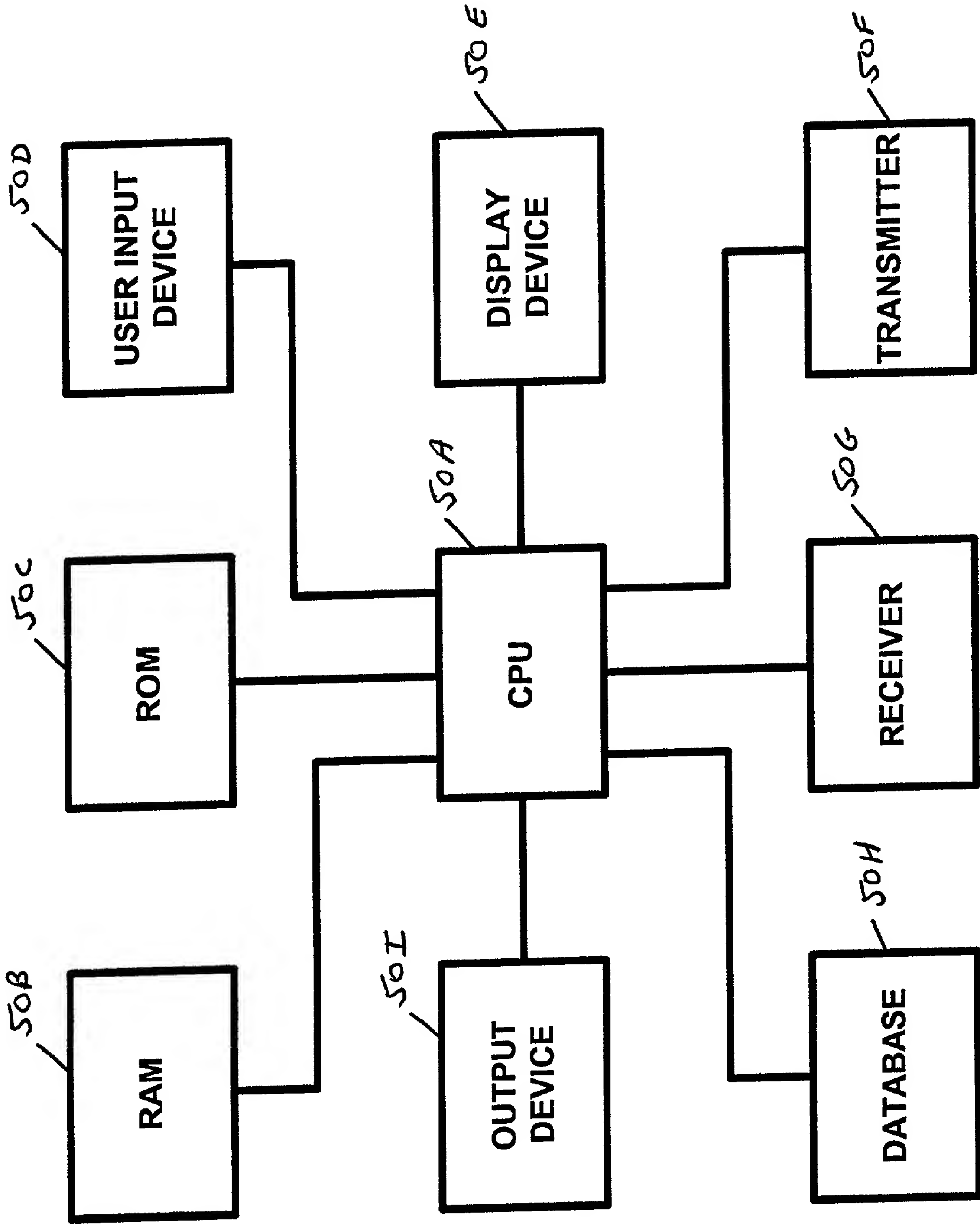
300

FIG. 4



400

FIG. 5



500

FIG. 6

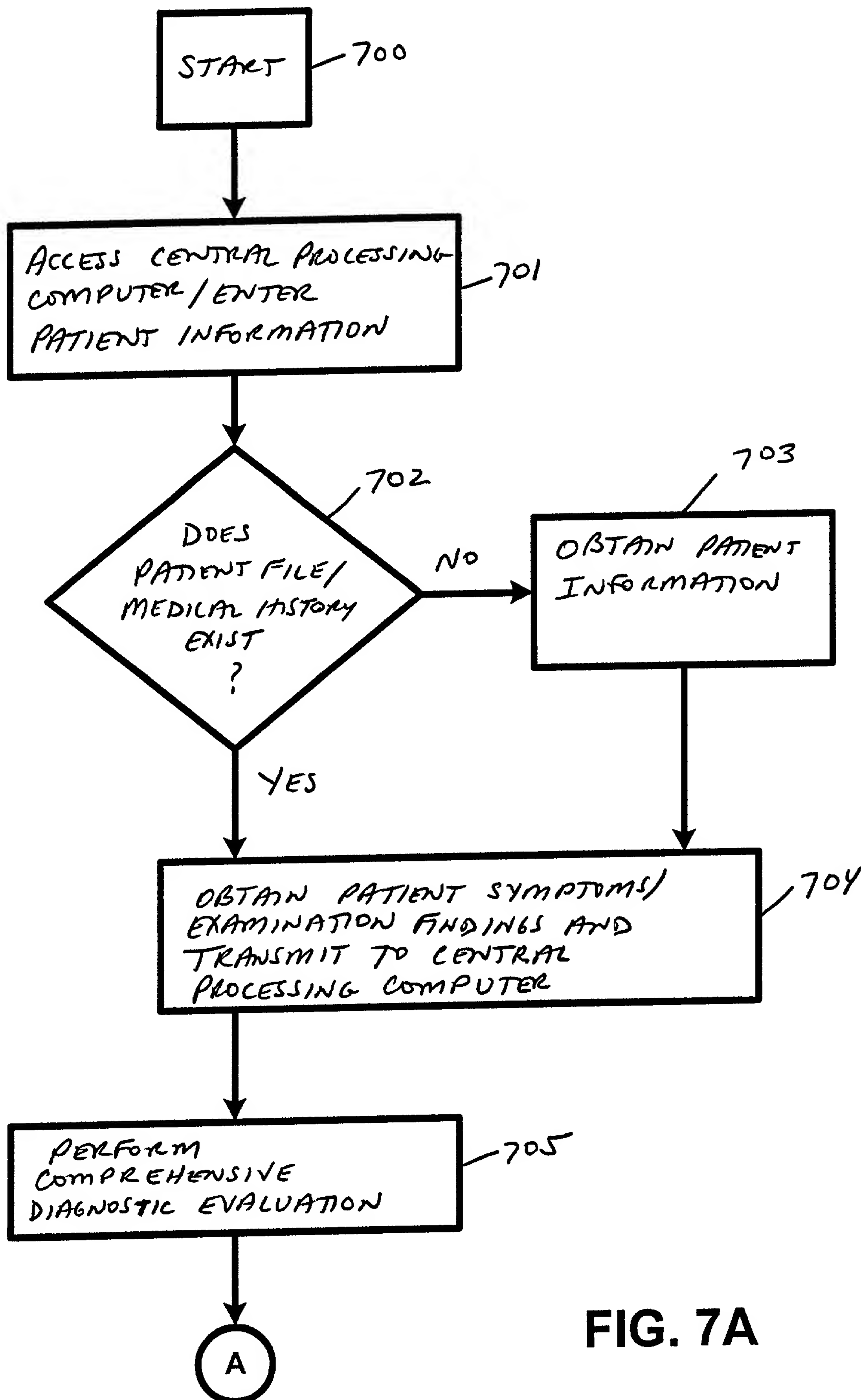


FIG. 7A

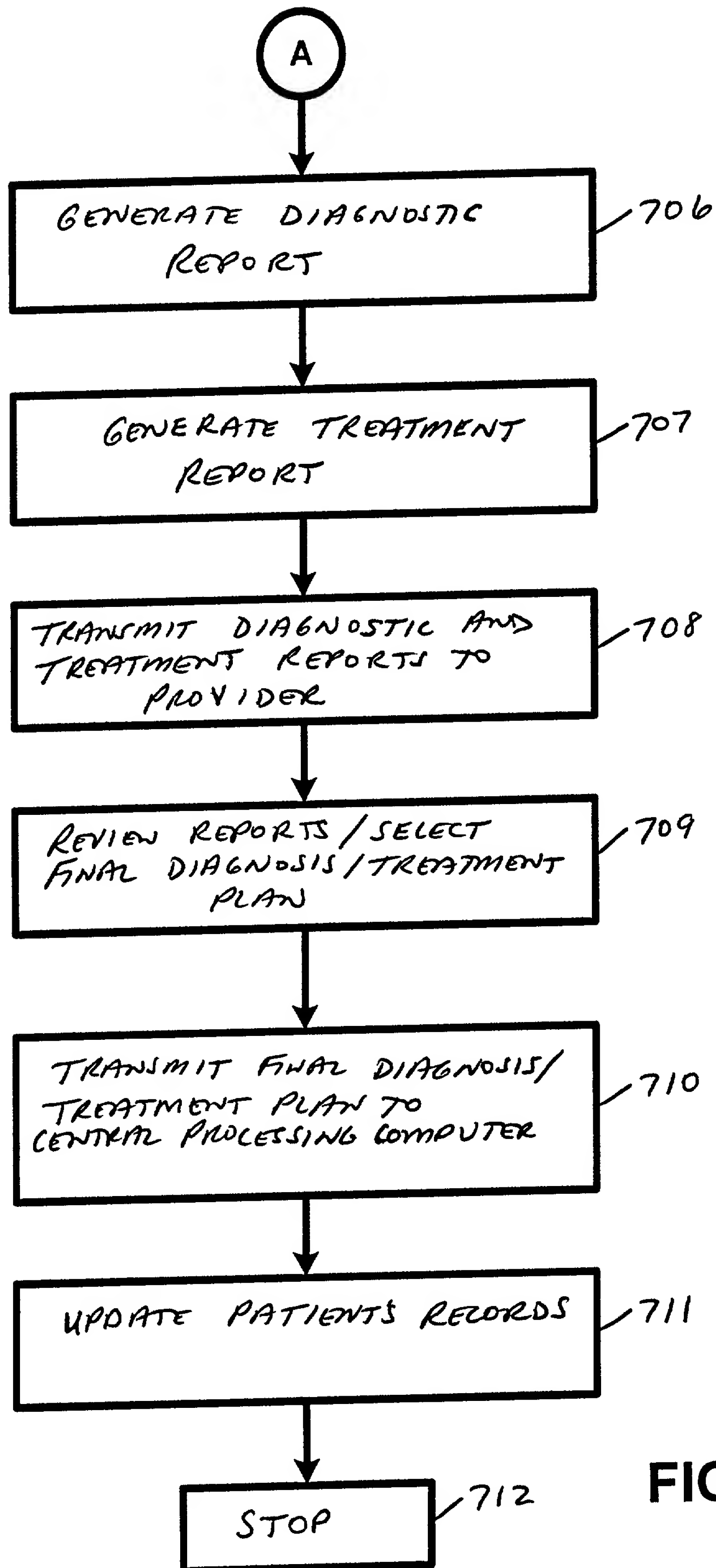


FIG. 7B

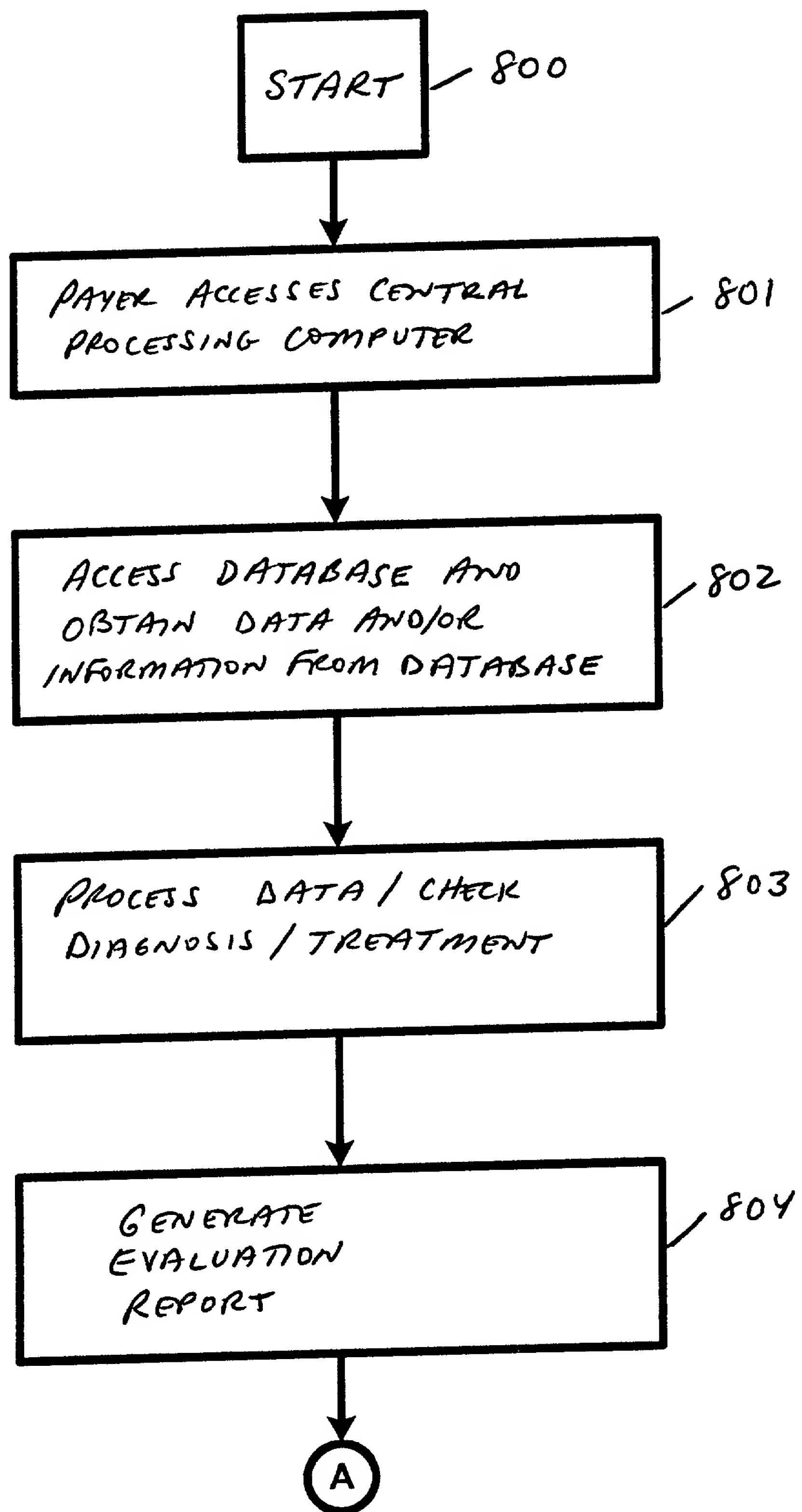
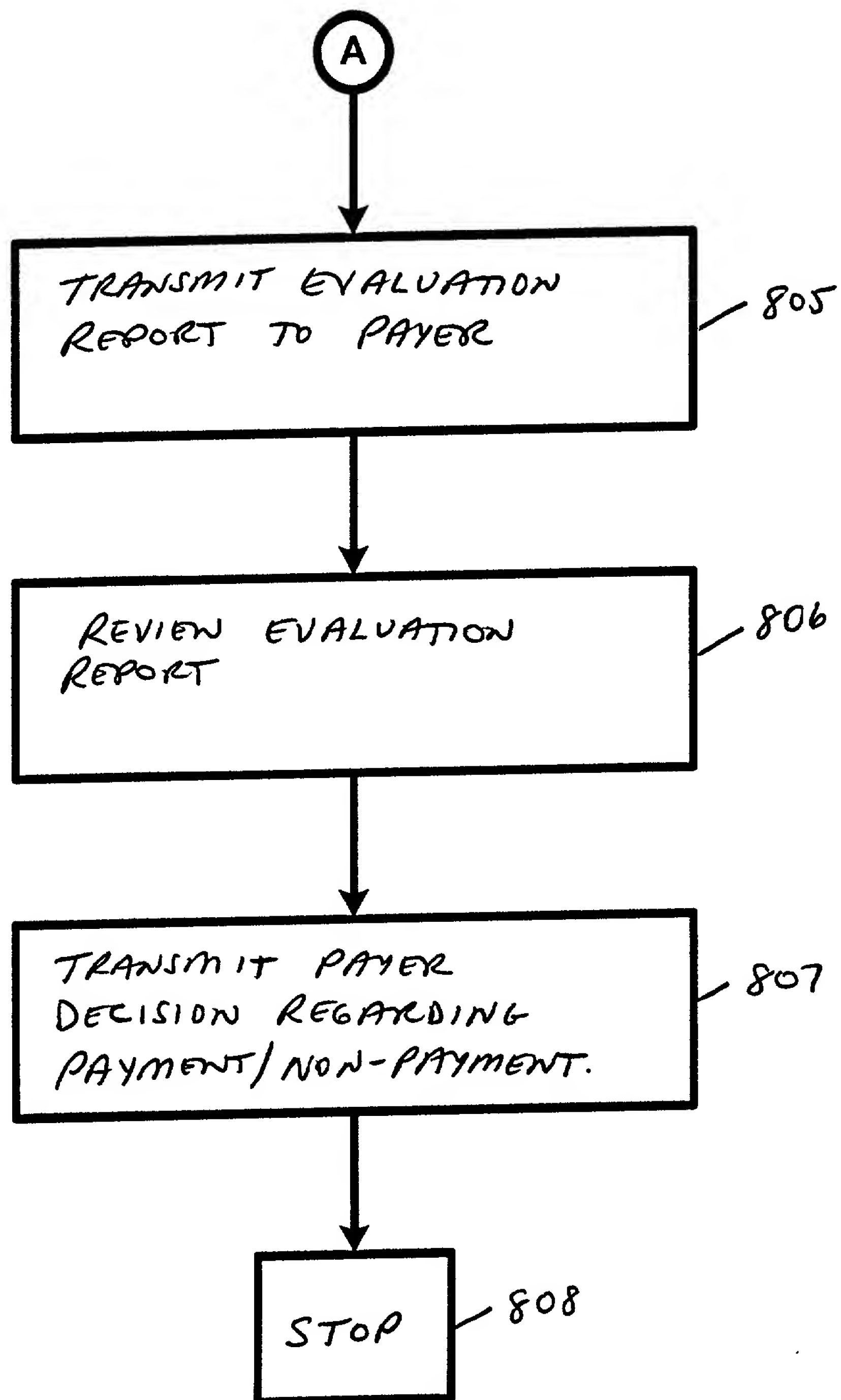


FIG. 8A



**FIG. 8B**

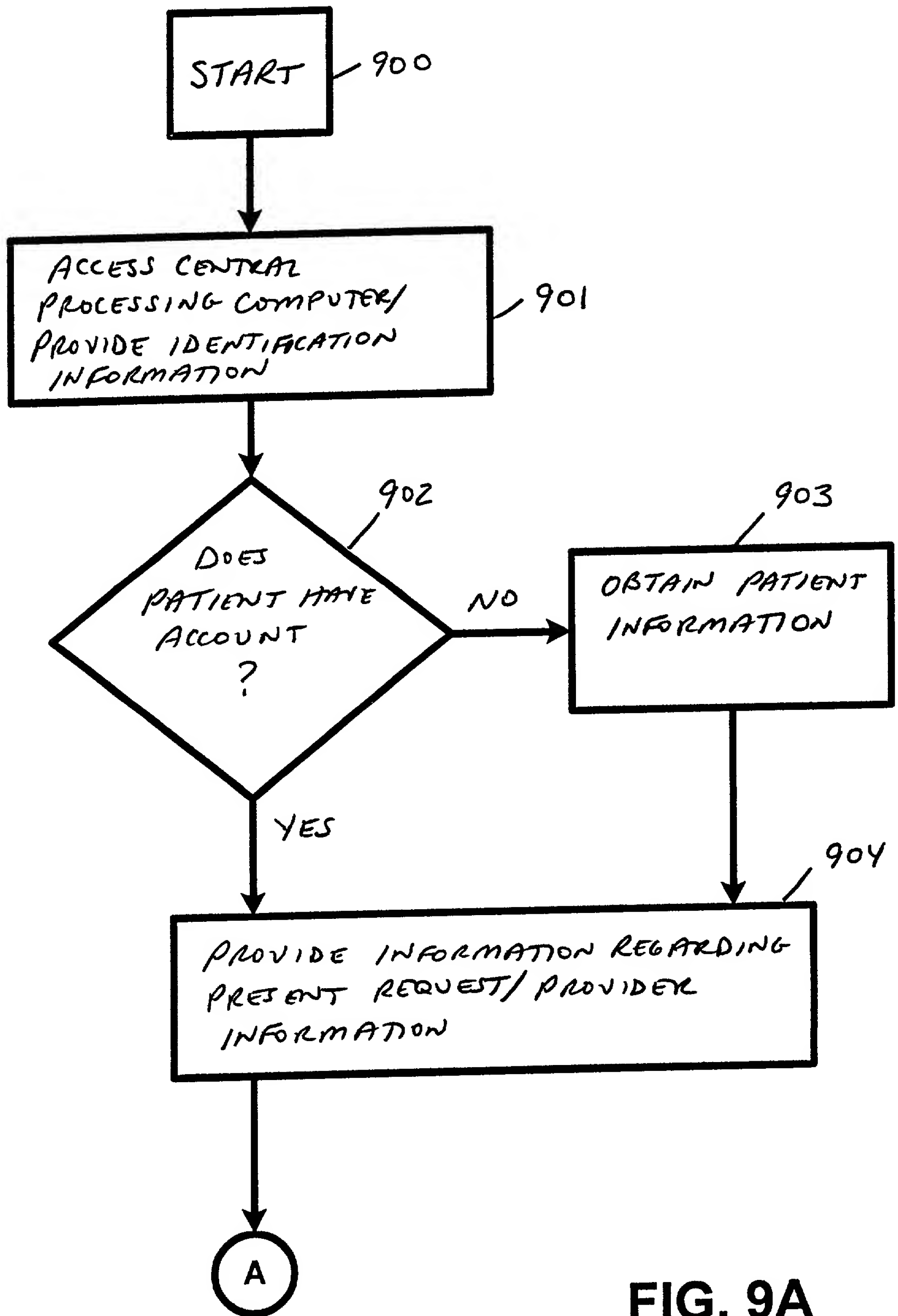


FIG. 9A

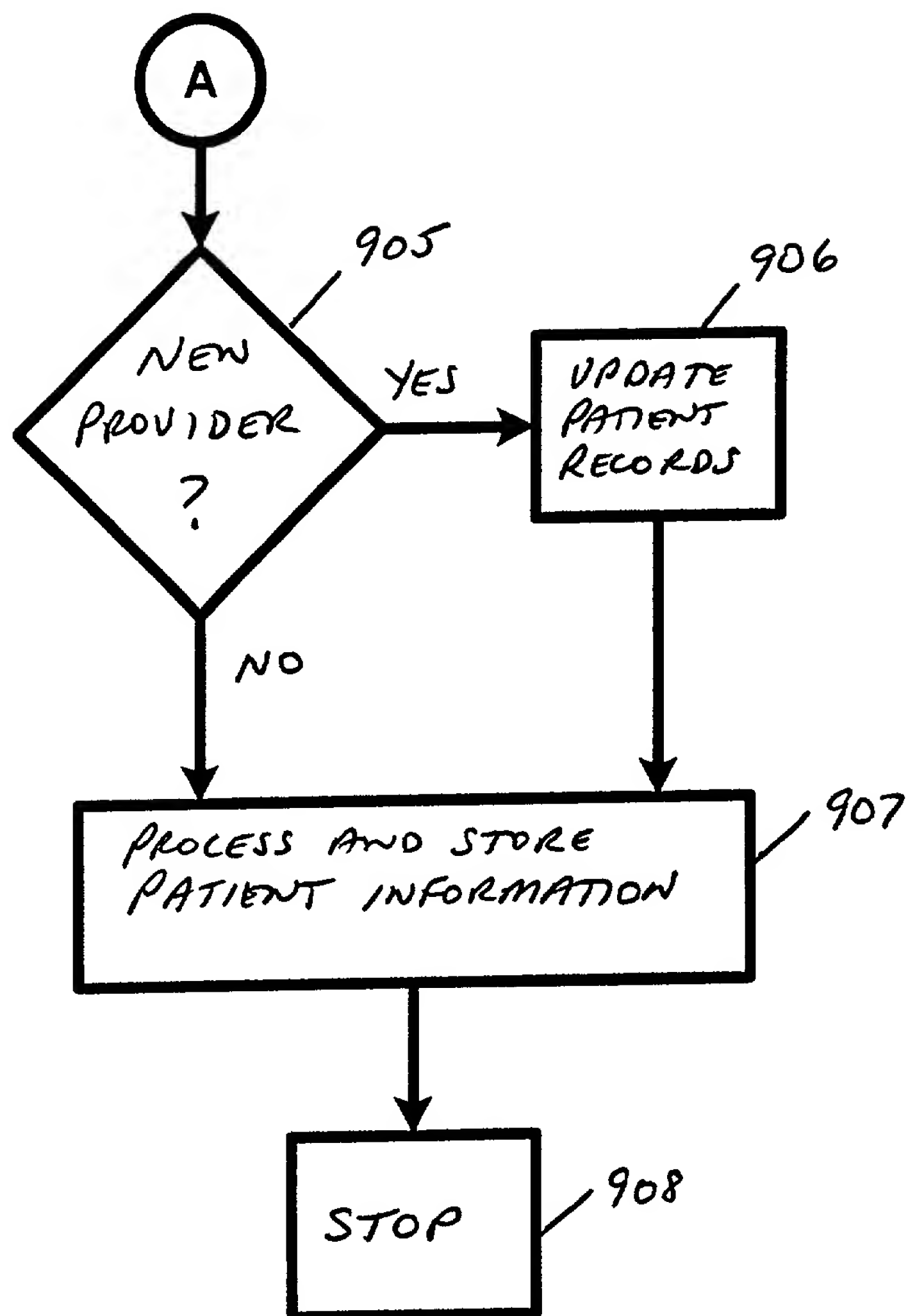


FIG. 9B

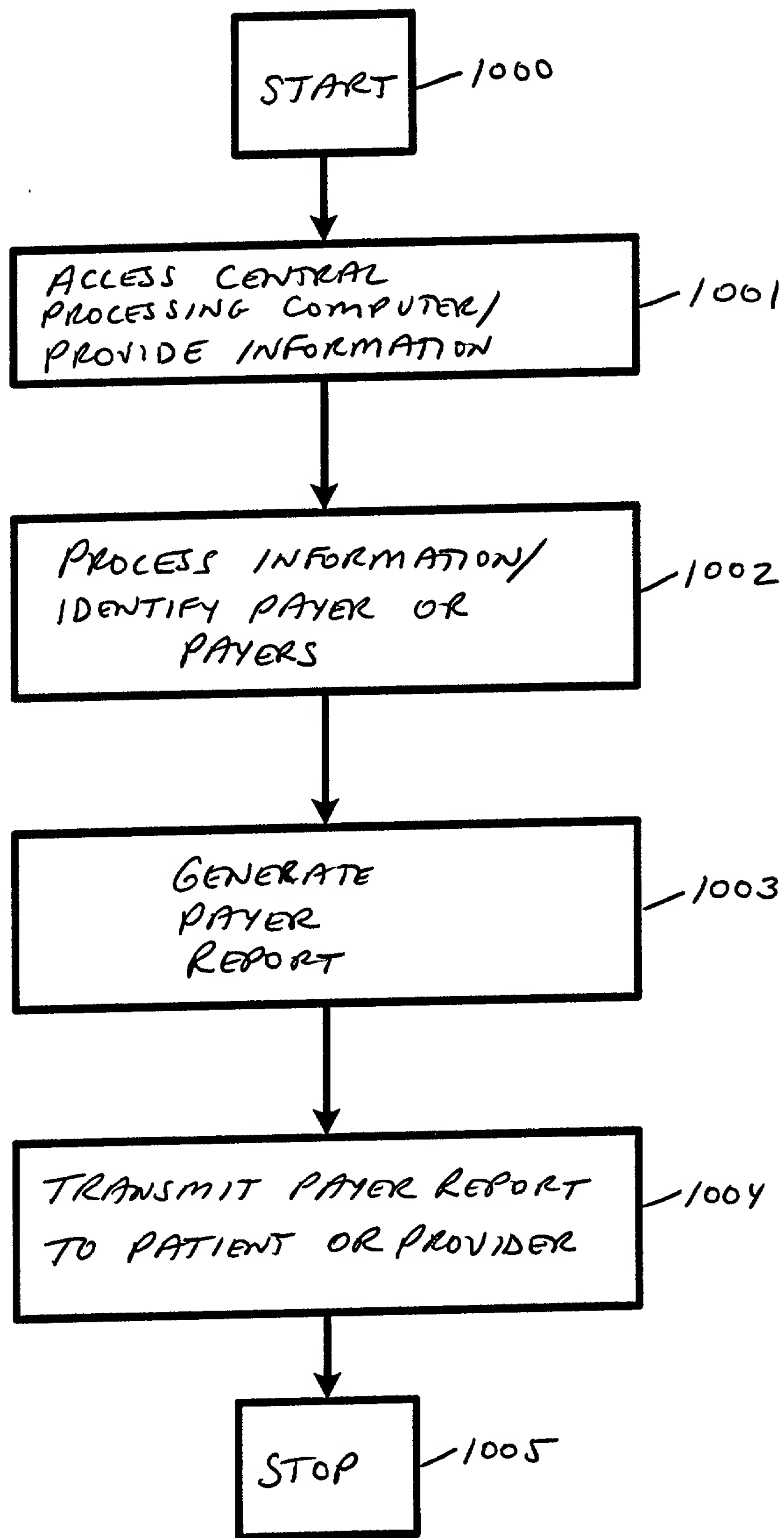


FIG. 10

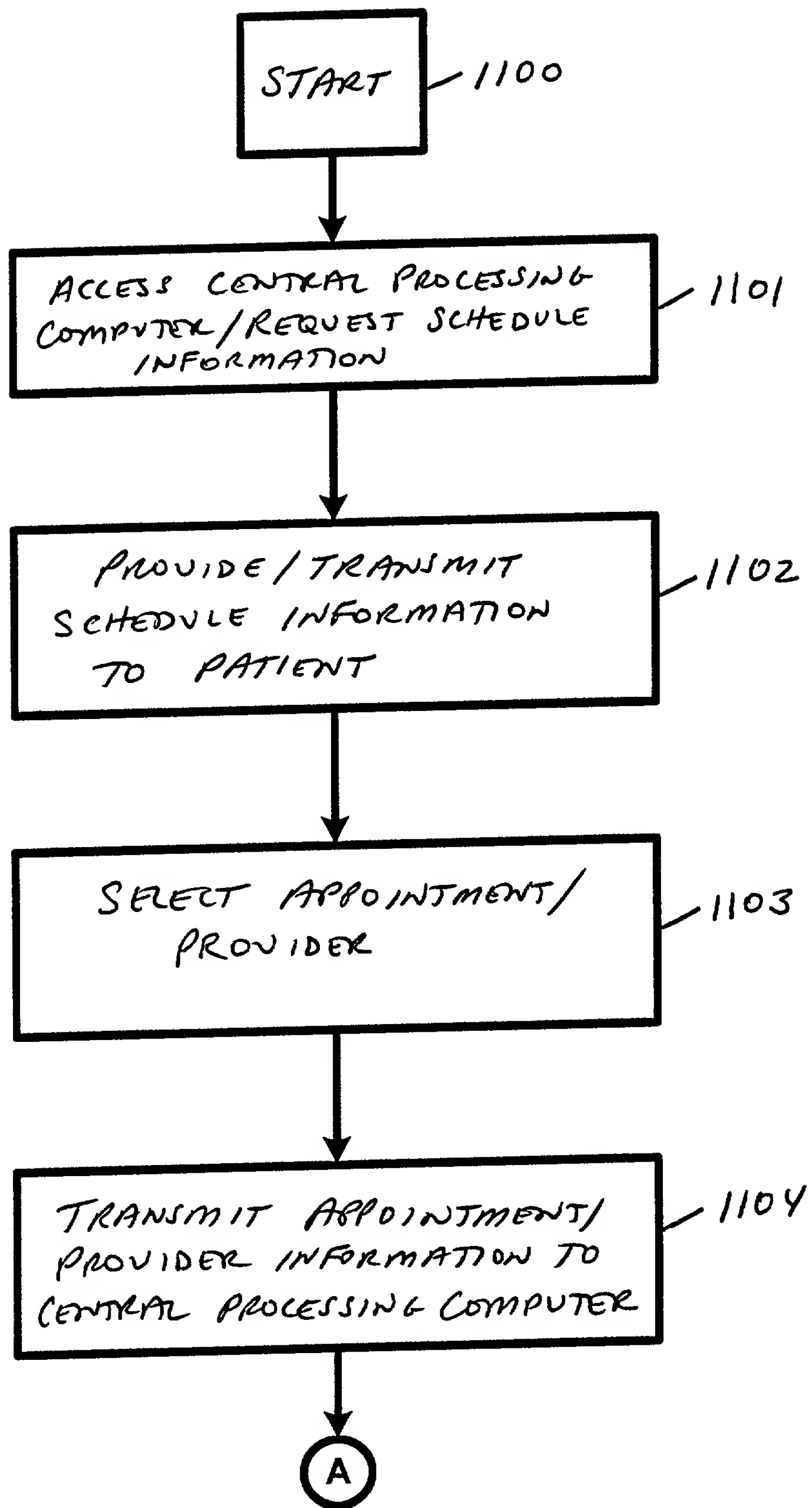
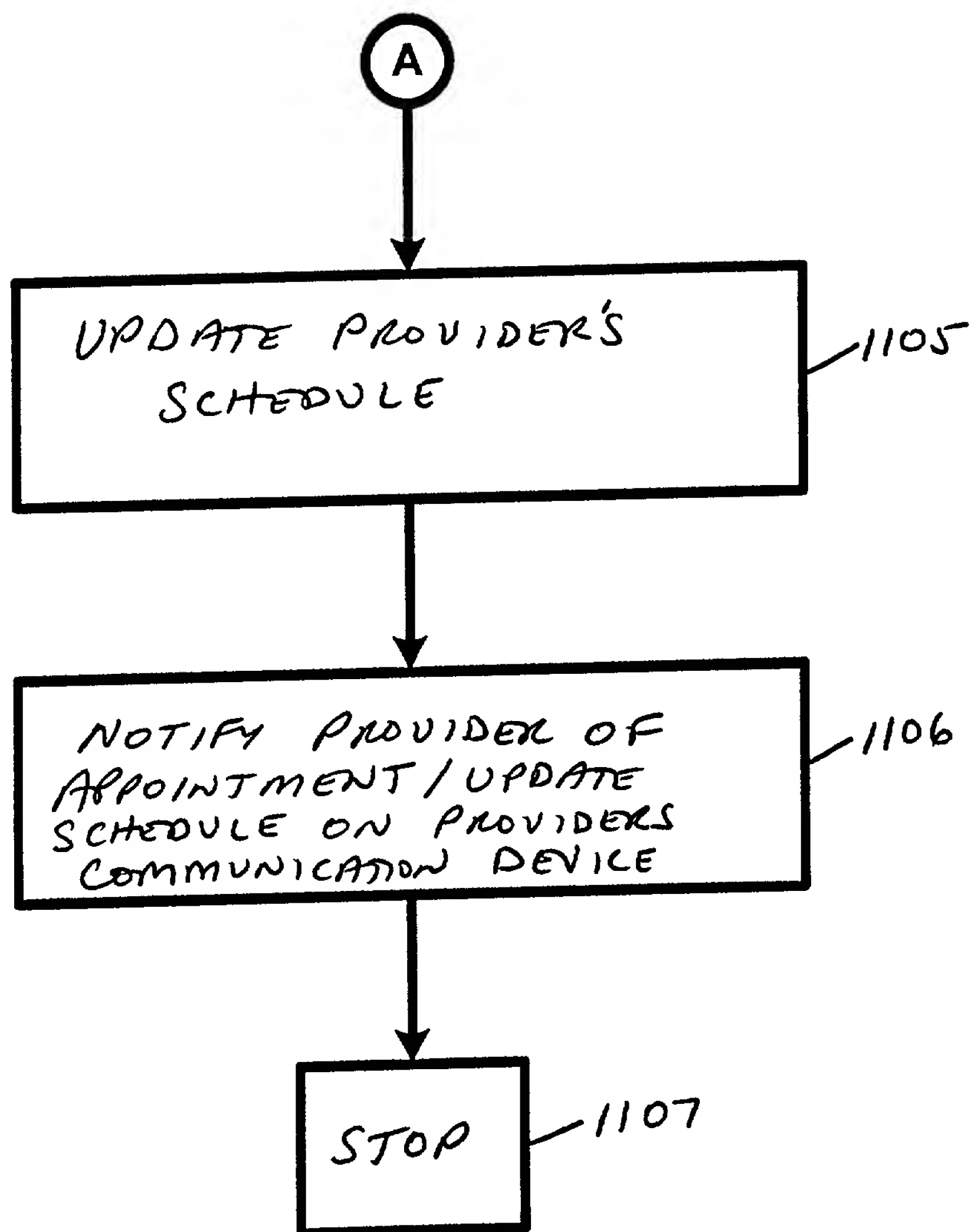


FIG. 11A



**FIG. 11B**

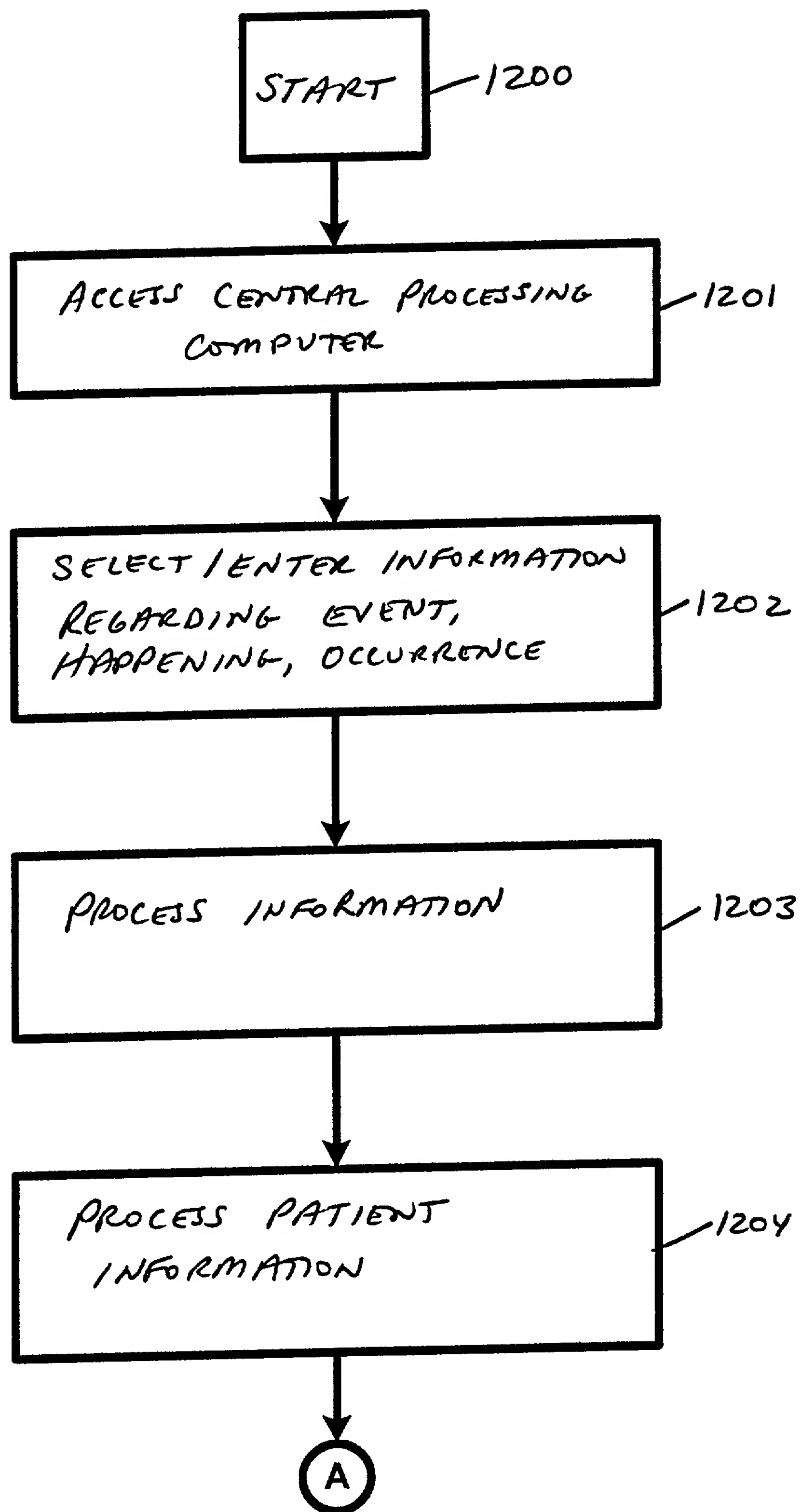


FIG. 12A

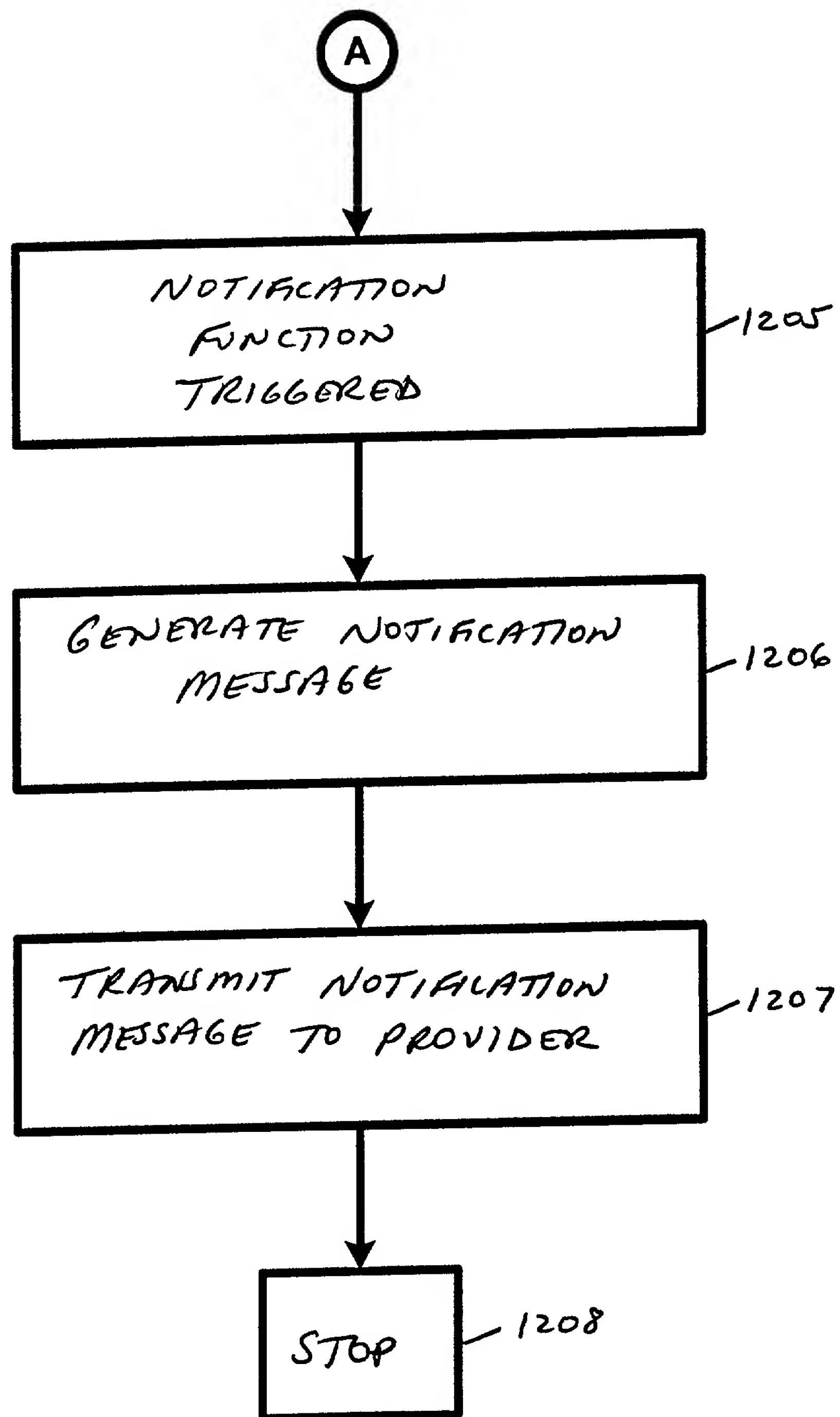


FIG. 12B

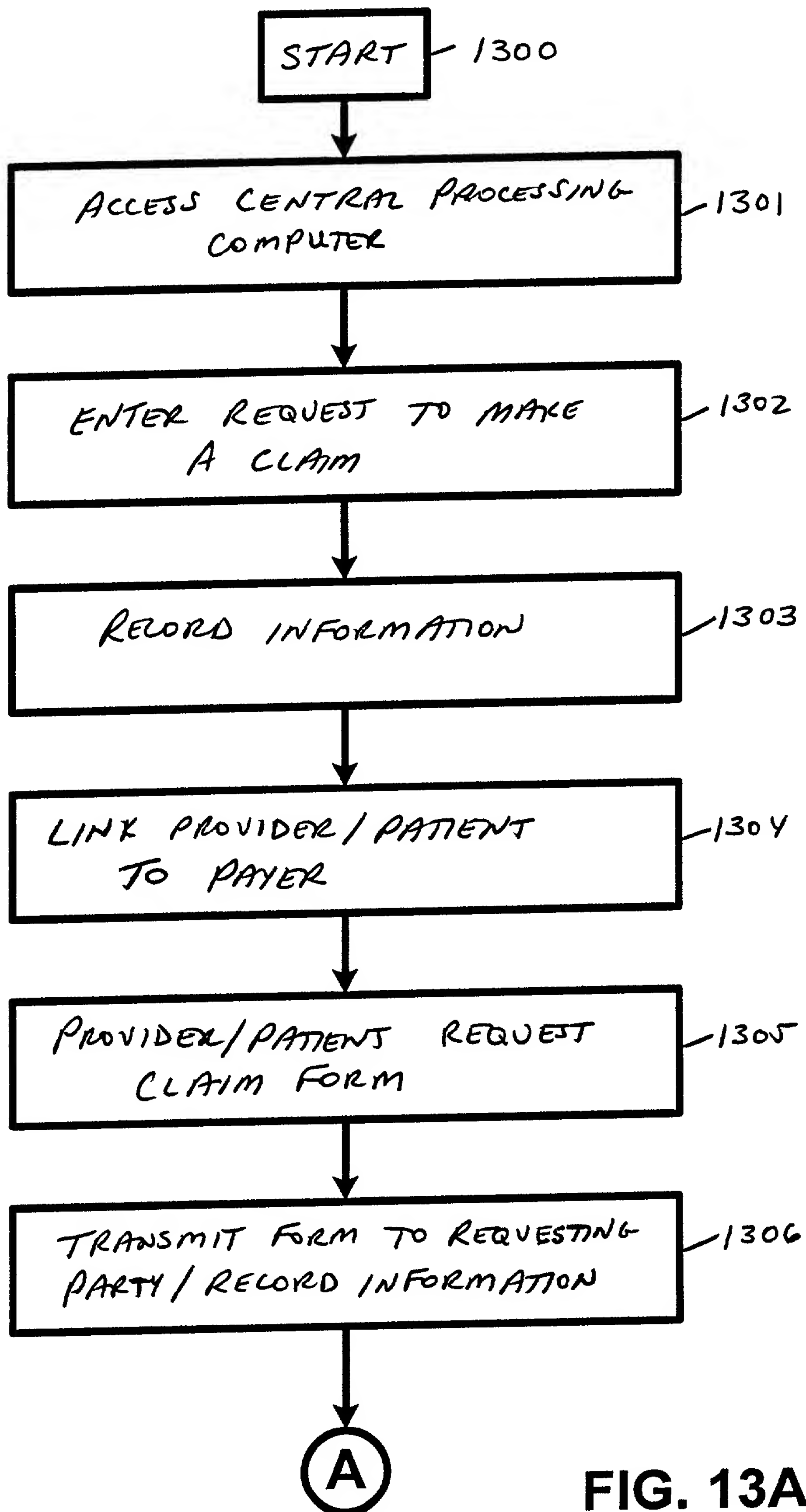


FIG. 13A

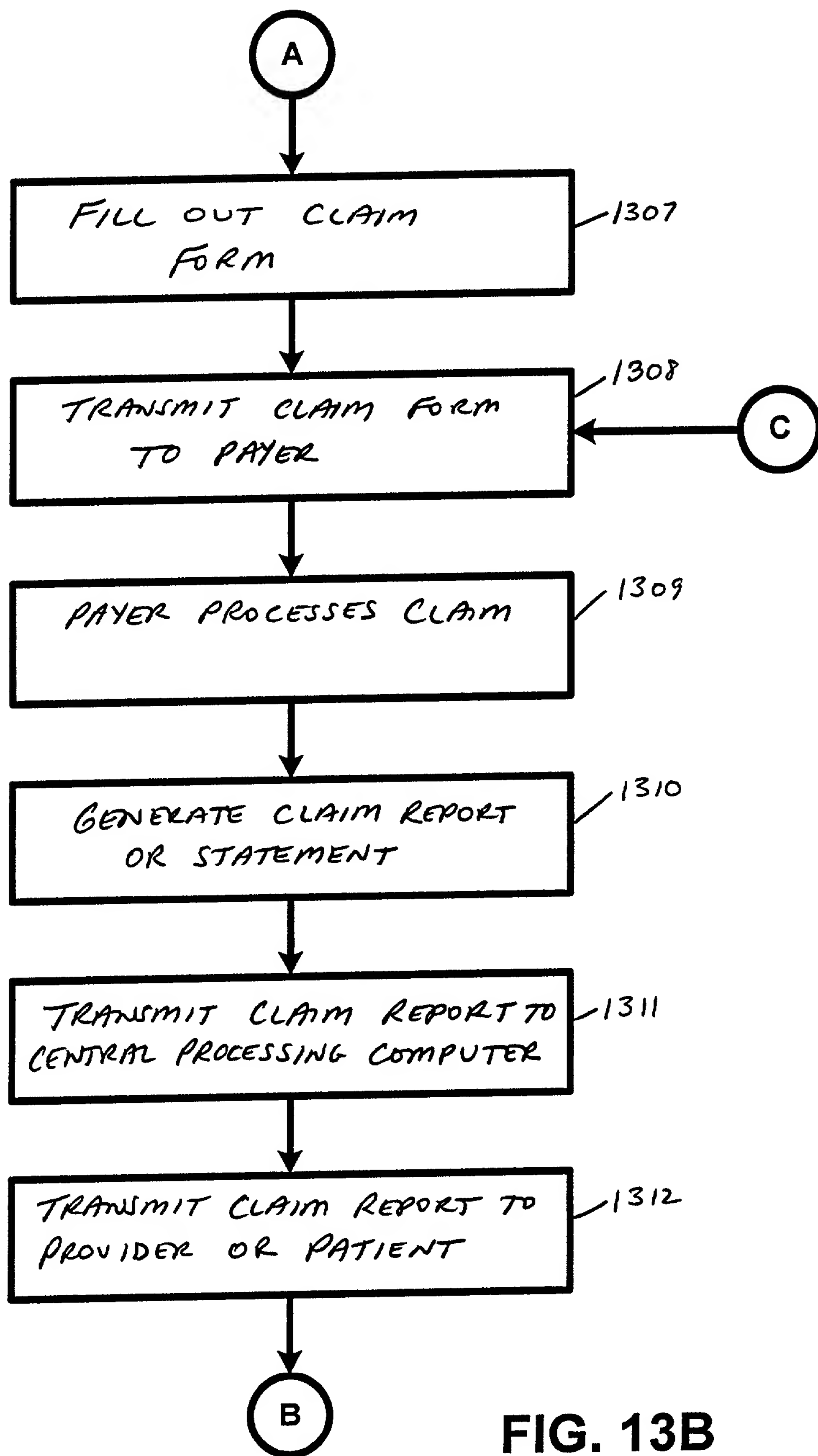
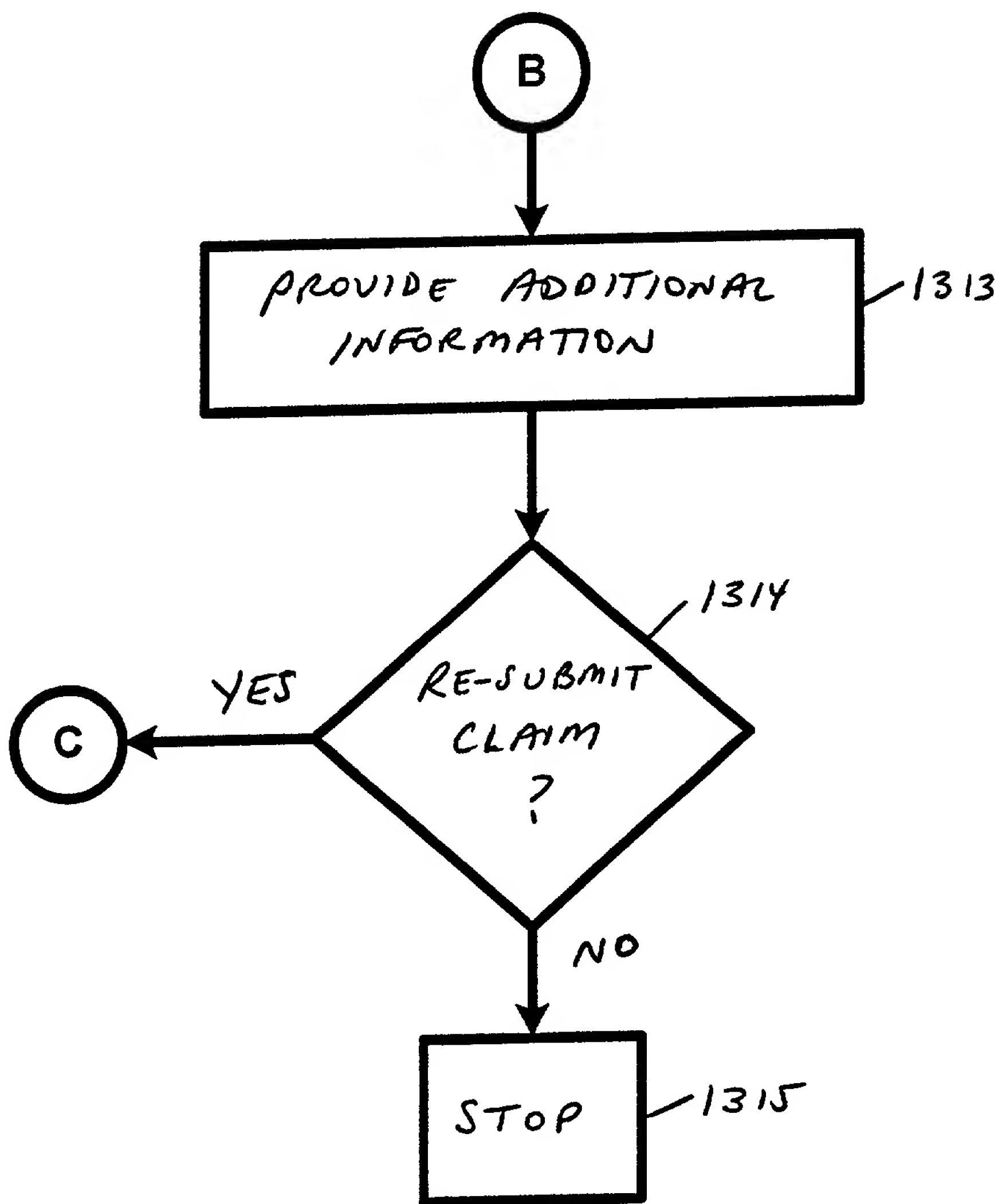


FIG. 13B



**FIG. 13C**

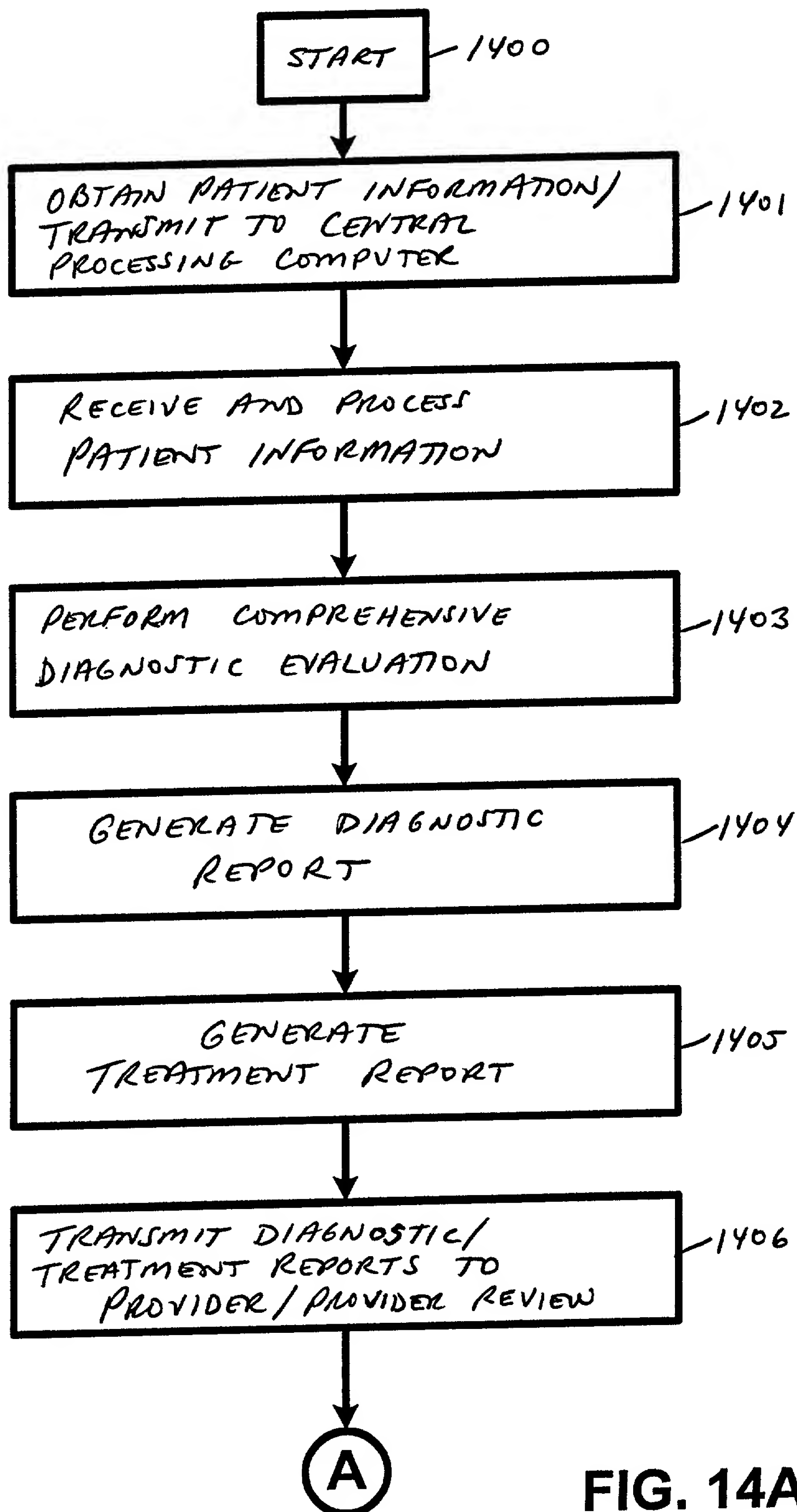


FIG. 14A

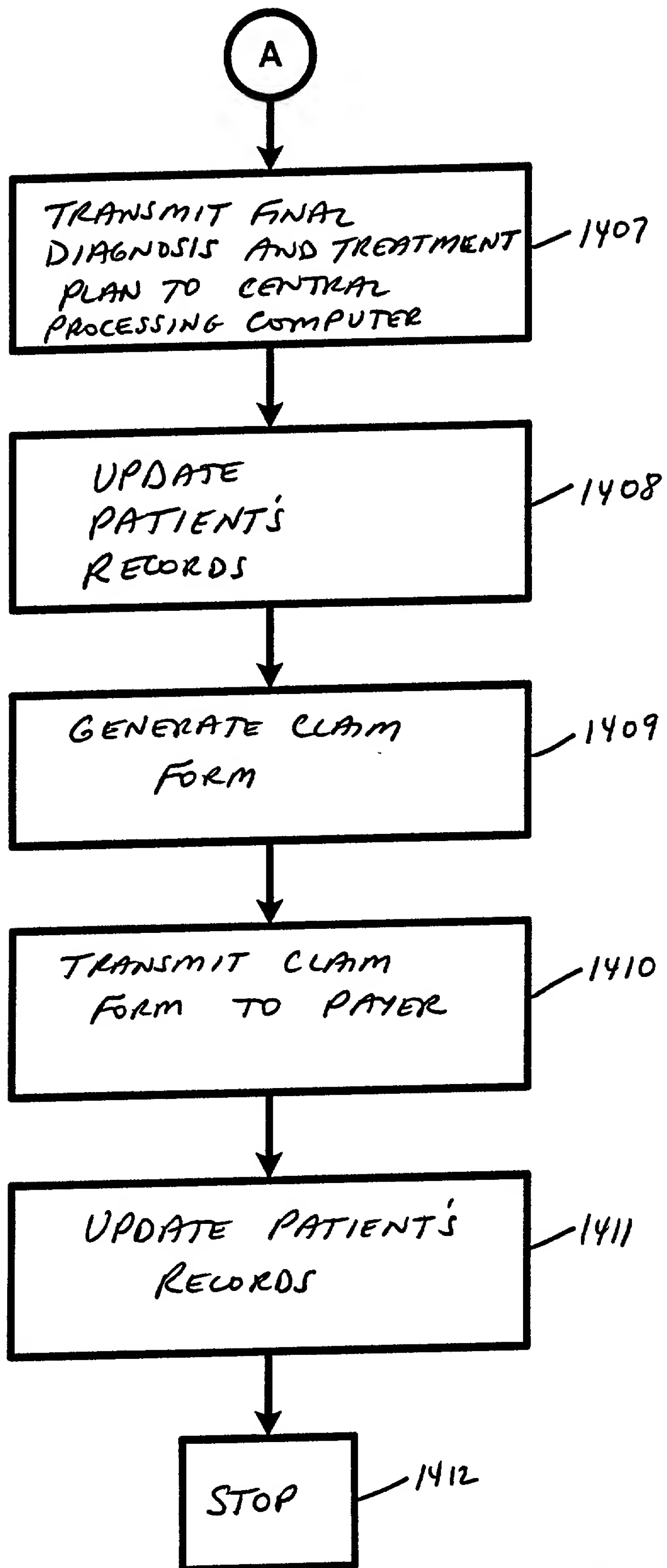


FIG. 14B

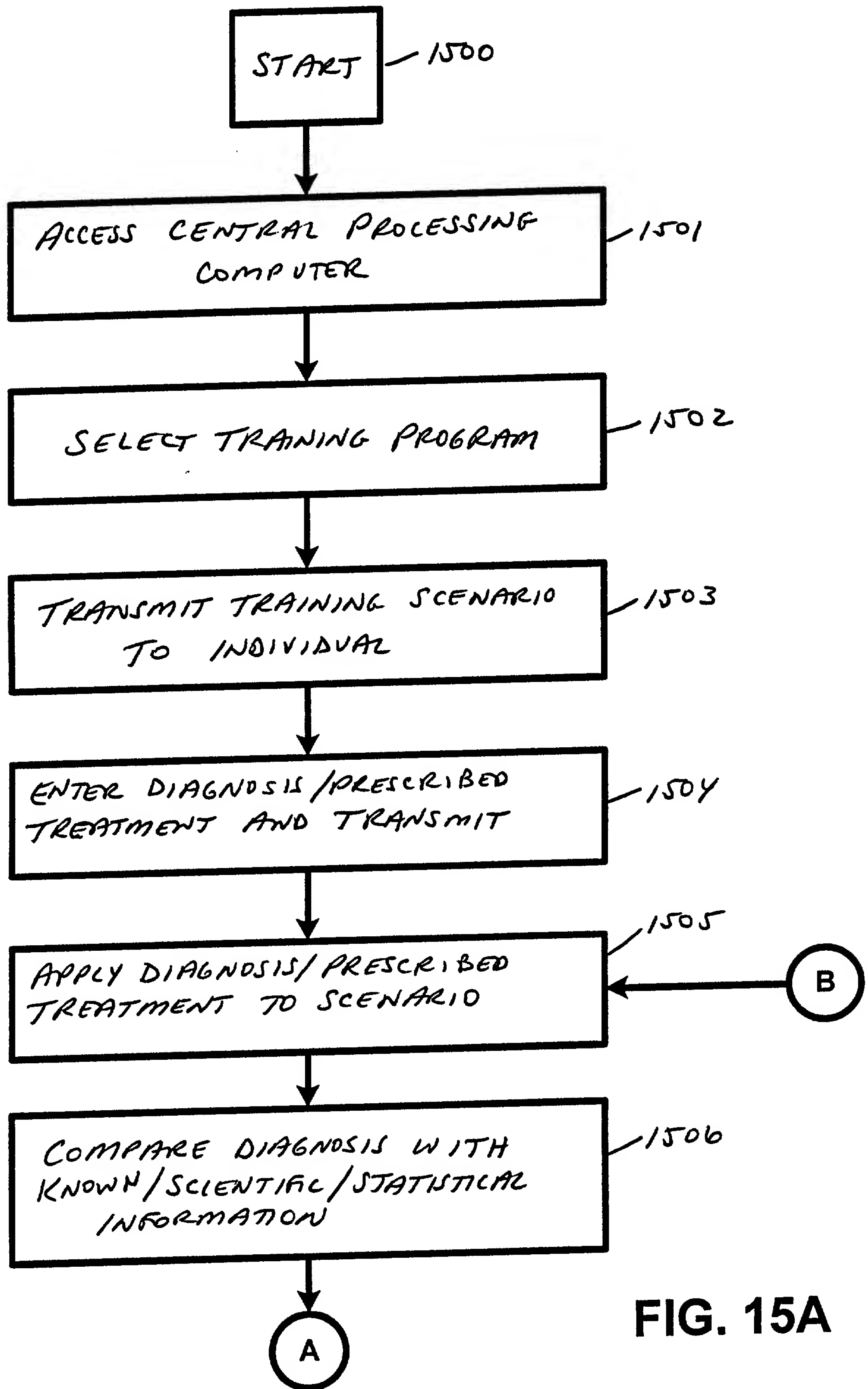


FIG. 15A

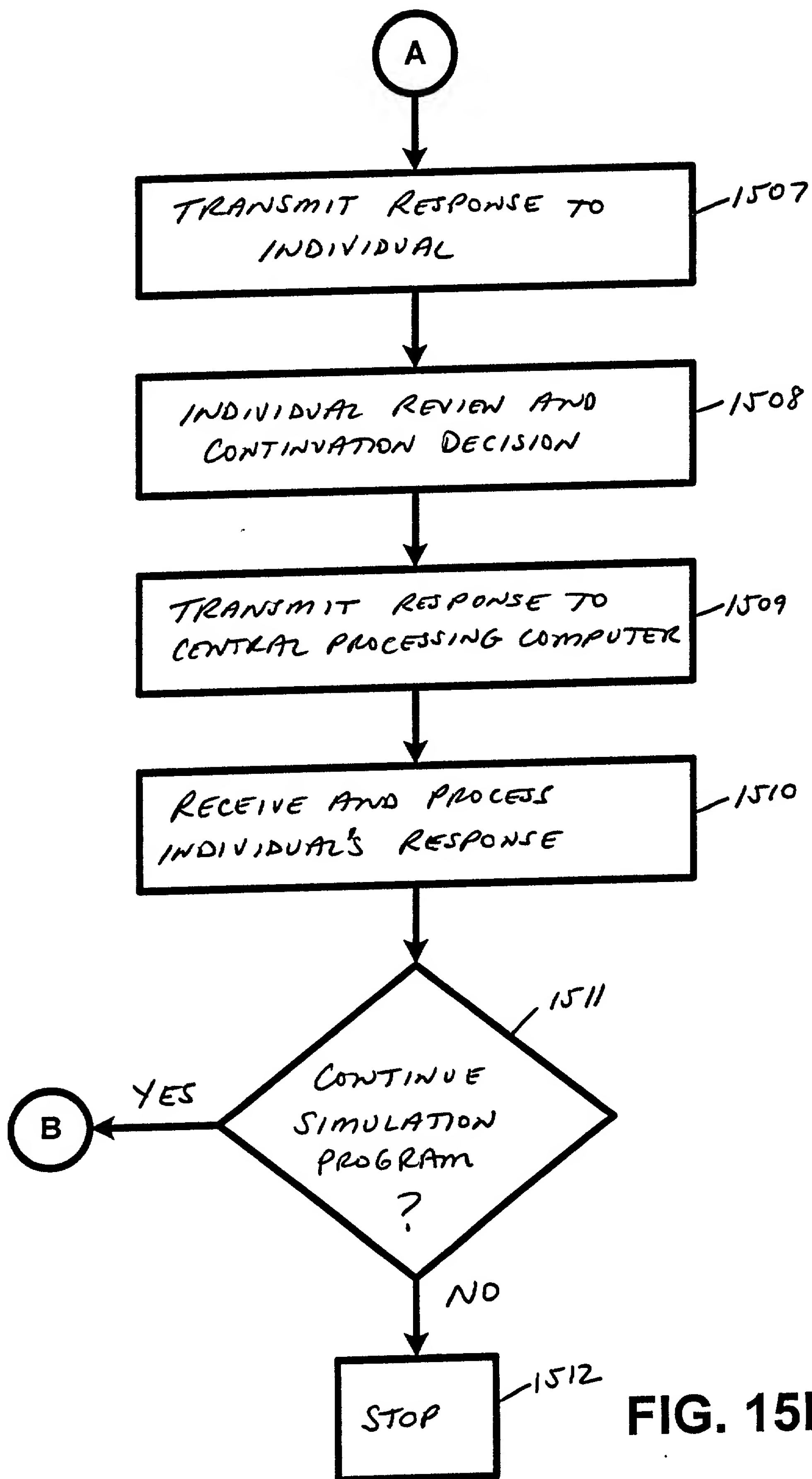


FIG. 15B